LISTING OF THE CLAIMS

A listing of all claims and their current status in accordance with 37 C.F.R. § 1.121(c) is provided below.

1. (previously presented) A method of soft-baking a semiconductor wafer substrate, comprising the acts of:

(a) soft-baking a substrate coated with a resist at a first temperature for a first predetermined period of time; and

(b) after act (a), soft-baking the substrate coated with the resist at a second higher temperature for a second predetermined period of time.

2. (Original) The method, as set forth in claim 1, wherein no resist craters are formed.

3. (Original) The method, as set forth in claim 1, wherein during the first predetermined period of time:

the resist hardens; and

the air trapped under the resist does not possess sufficient energy to expand through the resist.

4. (Original) The method, as set forth in claim 1, wherein during the first predetermined period of time:

the resist remains fluid;

air trapped under the resist expands through the resist to the surface; and

the resist flows back to its original conformal shape.

5. (Original) The method, as set forth in claim 1, wherein the semiconductor wafer is subjected to a temperature in the range of 30-90 °C during the first predetermined period of time.

6. (Original) The method, as set forth in claim 1, wherein the first predetermined period of time is less than 90 seconds.

7. (Original) The method, as set forth in claim 1, wherein the first predetermined period of time is more than 90 seconds.

8. (Original) The method, as set forth in claim 1, wherein the higher temperature is in the range of 90-150 °C.

9. (Original) The method, as set forth in claim 1, wherein the higher temperature is in the range of 100-130 °C.

10. (Original) The method, as set forth in claim 1, wherein the second predetermined period of time is less than 90 seconds.

11. (Original) The method, as set forth in claim 1, wherein the second predetermined period of time is more than 90 seconds.

12. (Original) A semiconductor wafer comprising a resist layer without craters at the completion of a two-part soft bake of the semiconductor wafer.

13. – 28. (Cancelled)